

III. Remarks

A. Claim Amendments

Claims 6 and 23 have been amended to more broadly recite that the shielding structure is “substantially” non-overlapping relative to the gate. Support for this amendment can be found at, for example, Page 7, second full paragraph.

B. Information Disclosure Statement

Applicants filed an information disclosure statement with the original application on September 29, 2003 but did not receive an initialed PTO Form 1449 with the present office action. Consideration of the references cited in the September 29, 2003 information disclosure statement and return of the initialed PTO FORM 1449 (modified) submitted therewith are requested.

C. Rejection under 35 U.S.C. §102

The Action rejects Claims 1-9 and 19-25 as being obvious from U.S. Patent No. 6,521,923 to D’Anna et al. (hereinafter, D’Anna) in view of U.S. Patent No. 6,372,557 to Leong. Reconsideration and withdrawal of this rejection are respectfully requested in view of the following arguments.

Initially, Applicants would like to note that it is unclear whether the Examiner is rejecting Claims 1, 8, 9, 19, 20, and 24 as being obvious from the cited combination or as being anticipated by D’Anna. For example, the Examiner characterizes the teachings of D’Anna in rejecting these claims, and then states that “D’Anna does not teach all the limitations of the claims.” Following this comment, the Examiner states that “in regards to claims 1 and 2, Leong teaches the device of claim 1, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.” Applicants

would like to point out that, for example, Claim 1 does not recite these features, hence Applicants' confusion as to whether the rejection of, for example, Claim 1 is an anticipation or obviousness rejection.

Notwithstanding the foregoing, Claim 1 is directed to an MOS device including, *inter alia*, at least one contact where the at least one contact comprises a **silicide layer** formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate. It is respectfully submitted that neither D'Anna nor the combination of D'Anna and Leong teaches an MOS device having this recited contact structure.

In rejecting Claim 1, the Examiner cites to Column 9, Lines 17-31 of D'Anna for providing this recited contact to the first source/drain region. This cited description from D'Anna provides that the **gate 60** of the device of D'Anna can comprise a sandwich structure including a bottom layer of highly doped polysilicon covered with a top layer consisting of a silicide. A silicided gate structure is clearly not "a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate." D'Anna does disclose that plug 74 (FIG. 3) can be a metal plug or a silicided plug, but FIG. 3 shows only a Tungsten metal plug. It is not apparent what is meant by "silicided plug." It is submitted that silicided plug may mean that only the top of plug 76 is silicided and thus that the silicided layer is not formed "on and in electrical connection with" at least a portion of the first source drain region as claimed in Claim 1. It may also be that the silicided plug is only formed adjacent to the source/drain region and that the source/drain region is coupled to the plug by a metallization layer, and, therefore, that the silicided layer is not formed "on and in electrical connection with" at least a portion of the first source drain region as claimed in Claim 1.

The Examiner's first citation to Leong is to Column 5, Lines 54-59 (Claim 1). This portion of Leong merely provides that an electrical contact is provided from the source region to the bottom of the substrate. Turning to the full disclosure of Leong, like D'Anna, Leong teaches

that the polysilicon gate structure 110 can be silicided but provides no teaching with respect to forming silicided contacts on the source/drain regions. With respect to contacts formed to the source/drain regions, Leong teach that metallization layers 136 and 136a are provided. (Column 4, Lines 17-27). The metallization layers “**can be gold or aluminum with silicon and/or copper doping.**” (Column 4, Lines 20-21) (Emphasis added). Simply, these layers are not contacts including a silicide layer, i.e., silicon doping is not the formation of a silicide.

For at least these reasons, it is submitted that Claim 1 is neither anticipated by nor obvious from the cited references and is, accordingly, allowable. Claims 2-9 depend from Claim 1 and are, therefore, also allowable.

Claim 19 is directed to an integrated circuit device having a plurality of MOS devices formed therein an including the silicide contact structure analyzed above in connection with Claim 1. For at least the reasons set forth above in connection with Claim 1, it is submitted that Claim 19, and Claims 20-25, which depend from Claim 19, are allowable over the cited references.

Reconsideration and withdrawal of the rejection of these claims are respectfully requested.

D. New Claims

New Claims 26-34 have been added. Examination and allowance of these claims are respectfully requested.

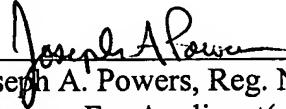
IV. Conclusion

In view of the foregoing remarks and amendments, Applicant(s) submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account 04-1679.

Respectfully submitted,

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